

## An ADC Design for Hearing AIDS with High Dynamic Range

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### ABSTRACT

This paper presents a high dynamic range oversampling analog-to-digital converter. The modulator has topology of cascade of integrator with multiple feedback (CIFB) second order with 3-bit quantizer delta-sigma modulator. The modulator noise transfer function is optimized for maximum quantization noise suppression. While the maximum out-of-band gain (OBG) of 2 considered for in-band noise shaping. The signal transfer function is like low-pass behavior. Due to multi-bit quantizer the higher stability achieved. The poles of the NTF lies inside the unit circle in z-domain. The zeroes and poles effect of the NTF are discussed for accurate noise shaping. The zeroes of the NTF, which are poles of the loop filter needs to be at the DC on the unit circle without NTF zero optimization technique. The modulator can achieve higher performance by NTF zero optimization technique. The poles of the NTF, which are zeros of the loop filter lies inside the unit circle. The operational amplifier inside the loop filter optimized for higher performance. The non-idealities factors of the operational amplifier like limited DC gain modeled. Also, complete modulator non-idealities like thermal noise and flicker noise also modeled and simulated. The second-order modulator with 3-bit quantizer having an oversampling ration (OSR) of 128 can achieve signal-to-noise ratio (SNR) of 105 dB as with full-scale input of 900 mV.

**Keywords:** Analog-to-Digital Converter, STF, NTF, OBG, Delta-Sigma.

### 1. INTRODUCTION

signals. The modulator can achieve 16-bit resolution with an oversampling ratio of

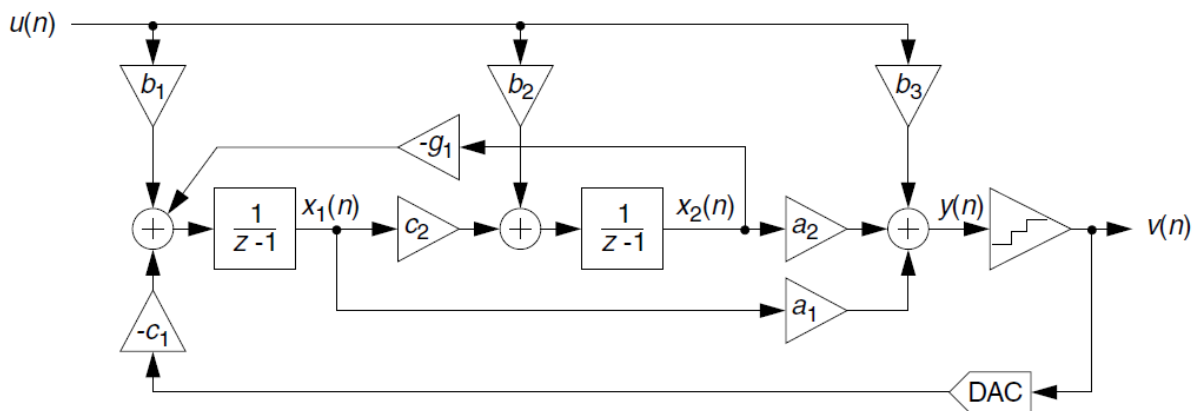


Figure 1: Block diagram of the CIFB topology

Recently, low power front-end circuit gaining popularity for biological signal monitoring and conversion. A second-order multi-bit delta-sigma modulator is modeled and simulated for hearing

128. The complete modulator circuit non-idealities like limited DC gain, limited slew-rate, thermal noise, and flicker noise, modeled and simulated. Due to small amplitude of the biological signal, quite challenging to process the signal

until converted to digital. The complementary metal oxide semiconductor (CMOS) allows to integrate the millions of transistors. The sensing activity of the analog circuit requires constant monitoring and further processing. Due to biological signal different bi-potential signal pose different challenges on the sensing and analog signal conversion. The requirement for biological analog signal to digital conversion is challenging in CMOS technology. Different analog-to-digital conversion (ADC) techniques are proposed, either successive approximation register (SAR) and delta-sigma modulator. A BioADC concept is proposed with 4-channel integrated bipotential ADC for electrocortical recording in 180 nm CMOS Technology. The proposed BioADC directly transduces microvolts biopotential into a digital form without need of power-hungry amplifier. The proposed design each channel consists of continuous-time first-order delta-sigma modulator using operational transconductance amplifier (OTA) input and current feedback path followed by a second-order comb-filter decimator with supply voltage of 1.5 V. The analog and digital circuits in each channel draw 2.1  $\mu\text{A}$  and 1.4  $\mu\text{A}$  of supply current, respectively. The bioADC can achieve an signal-to-noise-ratio (SNR) of 57 dB and signal-to-noise plus spurious-free dynamic range of 63.5 dB with effective number of bits 9-bit. It uses Gm-C structure for continuous-time integrator and utilizes the fully differential telescopic OTA. The common-mode control signal is derived using a standard circuit consisting of two differentials pairs. To maximizes noise and power efficiency of the OTA, the input pair operate in subthreshold and NMOS load are degenerated. To increase common-mode rejection ration (CMRR),

the bias voltages for output node are set as function of source coupled node voltage  $V_p$ . Also latched comparator is employed which operates in three stages, reset, amplify, and latch. During reset, the differential pair sets a small voltage difference across the reset switch that tracks the difference at the input. With a falling edge on reset, both reset and latch are low, and the differential pair with crossed coupled transistor load amplify the difference at the input. A rising edge on latch causes the cross-coupled inverters to amplify further and bring the outputs to supply rails. The micropower operation and direct digital readout make this circuit ideally suited for closed-loop neuromodulation application. [3]. To sense the bi-potential signal, a low-power and low-voltage delta-sigma modulator ADC design is proposed. It provides analog signal conversion to digital domain based on mixed clock-boosting/switched-opamp second-order delta-sigma modulator, which is capable of interfacing with several different types of signals existing in the human body, only by re-programming the output digital filter. The proposed modulator architecture employs a novel single-phase scheme technique, which improves the dynamic performance, and it also highly reduces the clocking circuitry complexity, substrate noise and area. The simulation results shows that the signal integrity can be preserved by exploring the gap between the high conductance region of PMOS and NMOS switches at much smaller supply voltage. The mixed clock-boosting and switched-opamp technique architecture together with overall distortion reduction results from using the proposed single-phase scheme, result that the dynamic range of the modulator is pushed closer to the theoretical limit of an ideal second-order modulator [4].

A continuous-time (CT) delta-sigma modulator proposed with dual-slope quantizer and pulse width modulation (PWM) DAC for bio-potential sensing applications. The proposed modulator quantizer and DAC operates in the time domain. The modulator has been implemented in 0.18  $\mu\text{m}$  CMOS technology with dynamic range (DR) of 83 dB for signal bandwidth of 256Hz. The proposed design can consume power of 13.3  $\mu\text{W}$  at supply voltage 1.4V with sampling frequency of 917kHz [5]. Another design that does modeling of a continuous-time modulator for bio-potential signal acquisition. The system level modeling shows that a third-order modulator can achieve SNR of 87.3dB for signal bandwidth of 20 kHz [6]. A high-resolution modulator for bio-potential signal monitoring is presented for three different modes of operation. A second-order feedforward modulator with 4-bit quantizer is selected according to analytic power optimization. A programmable sampling capacitor for the first integrator and novel reconfigurable power gated OTA to adjust power consumption in each operation mode. Also, an asynchronous embedded SAR converter implements low-power quantization and passive addition in the feed-forward topology. The proposed modulator architecture allows to peak SNDR of 99dB to 75 dB for signal bandwidth spanning from 256Hz to 16 kHz in 0.18  $\mu\text{m}$  CMOS Technology operated at supply voltage of 1-V.

This paper proposed a A second-order multi-bit delta-sigma modulator is modeled and simulated for hearing signals. The modulator can achieve 16-bit resolution with an oversampling ratio of 128. The complete modulator circuit r. idealities like limited DC gain, limited slew-rate, thermal noise, and flicker noise, modeled and simulated.

After the introduction, the second section discusses the second-order modulator with third section describes the simulation of the operation of the modulator. Finally, the paper.

## 2. MODULATOR TOPOLOGY

A modulator with CIFF topology and single-bit quantization is modeled using Delta-Sigma Toolbox [7] as shown in Figure 1. Due to CIFF topology the signal-transfer-function (STF) will have peaking issues but have advantage of low-power operational amplifier can be used for integrator as the signal swing inside the loop filter is small. The CIFF second-order modulator with NTF zero optimization technique can achieve signal-to-noise ratio of 87 dB with OSR of 128 with an OBG of 2. The modulator with CIFF topology coefficients is obtained from [18] shown in Table I.

Figure 2: STF and NTF plot (CIFF) shows the magnitude of the signal transfer function (STF) and noise transfer function (NTF) versus normalized frequency. The NTF plot shows a zero at the origin and a peak at the Nyquist frequency. The STF plot shows a peak at the Nyquist frequency.

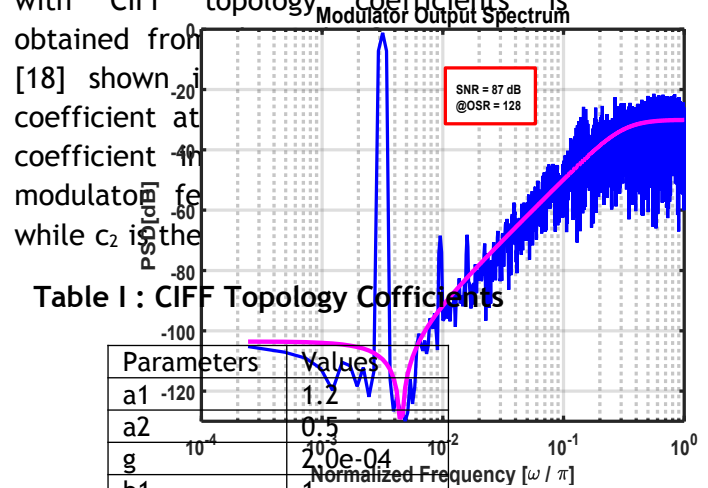
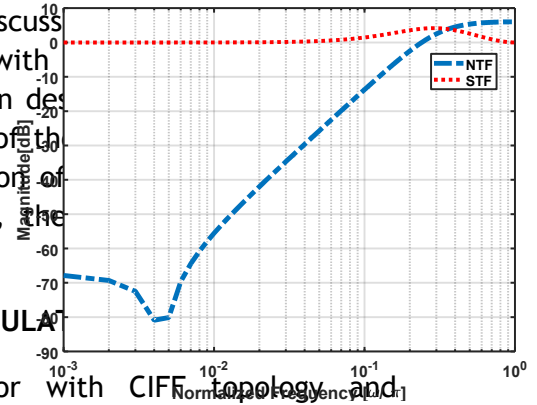


Table I : CIFF Topology Coefficients

Parameters	Values
a1	-120
a2	0.5
g	2.0e-04
b1	1
b2	0
b3	1
c1	1
c2	1

Figure 3: Output PSD plot (CIFF)

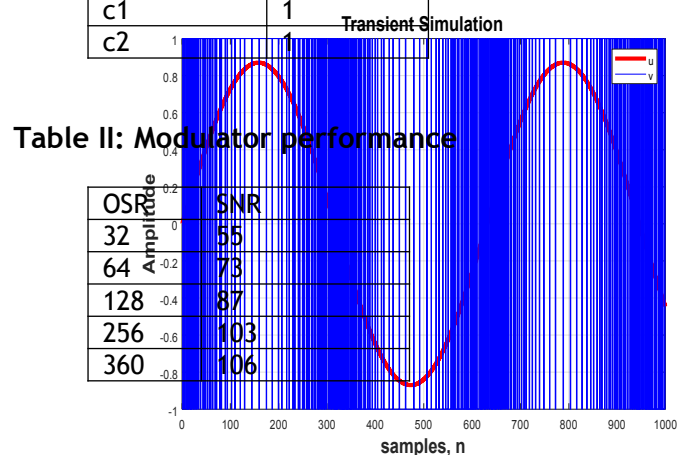


Table II: Modulator performance

OSR	SNR
32	55
64	73
128	87
256	103
360	106

Figure 4: Transient response

NTF zero optimization technique is implemented between the output of second integrator to the input of first integrator. The Table II shows the OSR versus SNR comparison, different plot. It is shown clearly that higher OSR will results in increased SNR. Figure 2 shows the NTF and STF plot with NTF zero optimization technique implemented shown. The STF clearly shows the peak effect with low-pass filter response as the modulator is low-pass. While the NTF shows the high pass filter response. The NTF response shows the quantization noise reduction from the signal band. The Figure 3 shows the output PSD plot for the modulator with OSR of 128 having SNR of 87 dB. The harmonic distortion can be observed very clearly in the output spectrum. The harmonic distortion is out-of-band which mean it does not contribute for the signal band performance. The Figure 4 shows the transient output response, that shows pulse coded modulation (PCM) output. This also shows the noise shaping behavior is working inside the loopfilter. The operational amplifier inside two integrator assumed infinite DC gain, and higher slew-rate. This causes maximum quantization noises attenuation.

## 1. NONIDEALITIES SIMULTION

To realize the practical circuit implementation the modulator also simulated for circuit non-idealities like limited DC gain, limited slew-rate, these circuit non-idealities are simulated using SDToolbox [8]. The thermal noise, flicker noise and limited DC gain also simulated. The simulation shows the degraded performance as compared to the actual ideal simulated modulator performance parameters.

## 4. CONCLUSION

The modulator has topology of cascade of integrator with multiple feedback (CIFB) second order with 3-bit quantizer delta-sigma modulator. The modulator noise transfer function is optimized for maximum quantization noise suppression. While the maximum out-of-band gain (OBG) of 2 considered for in-band noise shaping. The signal transfer function is like low-pass behavior. Due to multi-bit quantizer the higher stability achieved. The poles of the NTF lies inside the unit circle in z-domain. The zeroes and poles effect of the NTF are discussed for accurate noise shaping. The zeroes of the NTF, which are poles of the loop filter needs to be at the DC on the unit circle without NTF zero optimization technique. The modulator can achieve higher performance by NTF zero optimization technique. The poles of the NTF, which are zeros of the loop filter lies inside the unit circle. The operational amplifier inside the loop filter optimized for higher performance. The non-idealities factors of the operational amplifier like limited DC gain modeled. Also, complete modulator non-idealities like thermal noise and flicker noise also modeled and simulated. The second-order modulator with 3-bit quantizer having an oversampling ration (OSR) of 128 can achieve signal-to-noise ratio (SNR) of 105 dB as with full-scale input of 900 mV.

## 5. ACKNOWLEDGMENT

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